

**In the Claims:**

Please amend claims 13, 18, 19, 24, and 27, add claims 32-37 and cancel claim 17 as follows:

1 - 12. (canceled).

13. (currently amended): A method for encapsulating a solder joint between an integrated circuit chip and a substrate, comprising the steps of:

providing a substrate including a surface thereon having a plurality of electrical conductors positioned on the surface;

providing an integrated circuit chip located above the surface of the substrate to form a gap between a bottom side of the chip and said surface of the substrate, wherein a plurality of conductive leads project from lateral sides of said integrated circuit chip, said lateral sides not including said bottom side;

forming a solder joint for electrically connecting each conductor with the conductor's respective lead;

forming a composition that includes a photoinitiator, a dispersed phase of particulate silica filler, and a resin precursor, wherein the filler has a particle size of 31 microns or less if the filler is silica, and wherein the resin precursor consists essentially of a cyanate ester monomer, a cyanate ester prepolymer, or a mixture of the monomer and prepolymer;

applying an amount of the composition at a thickness sufficient to cover substantially all of the solder joint; and

photocuring the composition to reinforce the solder joint, wherein photocuring the

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is independently selected from the group consisting of non-interfering alkyl, aryl, alkaryl, heteroatomic, heterocyclic, carbonyloxy, carboxy, hydrogen, C<sub>1-6</sub> alkyl, C<sub>1-6</sub> allyl, C<sub>1-6</sub> alkoxy, halogen, maleimide, propargyl ether, glycidyl ether and combinations thereof; A is selected from the group consisting of C<sub>1-12</sub> polymethylene, CH<sub>2</sub>, dicyclopentadienyl, aralkyl, aryl, cycloaliphatic, CII(CII<sub>3</sub>), SO<sub>2</sub>, O, C(CF<sub>3</sub>)<sub>2</sub>, CII<sub>2</sub>OCH<sub>2</sub>, CH<sub>2</sub>SCII<sub>2</sub>, CII<sub>2</sub>NHCH<sub>2</sub>, S, C(=O), OC(=O), OCOO, S(=O), OP(=O), OP(=O)(=O)O, alkylene radicals, C(CII<sub>3</sub>)<sub>2</sub>, and combinations thereof.

16. (previously presented): The method of claim 13, wherein the cyanate ester is selected from the group consisting of cyanatobenzene 1,3-and 1,4-dicyanatobenzene, 2-tert-butyl-1,4-dicyanatobenzene, 2,4-dimethyl-1,3-dicyanatobenzene, 2,5-di-tert-butyl-1,4-dicyanatobenzene, tetramethyl-1,4-dicyanatobenzene, 4-chloro-1,3-dicyanatobenzene, 1,3,5-tricyanatobenzene, 2,2',4,4'-dicyanobiphenyl, 3,3',5,5'-tetramethyl-4,4'-dicyanobiphenyl, 1,3-dicyanatonaphthalene, 1,4-dicyanatonaphthalene, 1,5-dicyanatonaphthalene, 1,6-dicyanatonaphthalene, 1,8-dicyanatonaphthalene, 2,6-dicyanatonaphthalene, 2,7-dicyanatonaphthalene, 1,3,6-tricyanatonaphthalene, bis(4-cyanatophenyl)methane, bis(3-chloro-4-cyanatophenyl)methane, 2,2-bis(4-cyanatophenyl)propane, 2,2-bis(3,5-dichloro-4-cyanatophenyl)propane, 2,2-bis(3,5-dibromo-4-cyanatophenyl)propane, bis(4-cyanatophenyl)ether, bis(p-cyanophenoxyphenoxy)-benzene, di(4-cyanatophenyl)ketone, bis(4-cyanatophenyl)thioether, bis(4-cyanatophenyl)sulfone, tris(4-cyanatophenyl)phosphite, tris(4-cyanatophenyl)phosphate and combinations thereof.

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17. (canceled).

18. (currently amended): The method of claim 13, wherein the filler silica comprises from about 40% to about 75% by weight of the composition.

19. (currently amended): The method of claim 18, wherein the filler silica includes fused silica and amorphous silica.

20. (canceled).

21. (previously presented): The method of claim 13, wherein a coefficient of linear thermal expansion of the cured composition is from about 26 to about 39 ppm/degree C.

22. (previously presented): The method of claim 13, wherein a glass transition temperature of the cured composition is from about 100 to about 160 degrees C.

23. (previously presented): The method of claim 13, wherein the composition includes from 1 to 20 parts of surface treating agents selected from the group consisting of vinyltrimethoxysilane, vinyltriethoxysilane, N(2-aminooctyl)3-aminopropylmethyldimethoxysilane, 3-aminopropylethoxysilane, 3-glycidoxypropyltrimethoxysilane, 3-glycidoxypropylmethyl dimethoxysilane and combinations thereof, based on 100 parts of the resin.

24. (currently amended): The method of claim 13, wherein the composition ~~further comprises a filler selected from the group consisting of Silica;~~ includes at least one of Aluminum Oxide, 92% Alumina, 96% Alumina, Aluminum Nitride, Silicon Nitride, Silicon Carbide, Beryllium Oxide, Boron Nitride and Diamond powder.

25. (canceled).

26. (canceled).

27. (currently amended): The method of claim ~~13~~, wherein the cured composition exhibits a coefficient of linear thermal expansion of about 26 ppm/ °C to less than about 39 ppm/ °C and a glass transition temperature between 100 °C and 160 °C.

28. (previously presented): The method of claim 13, wherein the resin precursor is a mixture of polyfunctional cyanate esters with at least one cyanate ester having hydroxy groups and radical-polymerizable unsaturated double bonds.

29. (previously presented): The method of claim 28, wherein a ratio of cyanato groups to hydroxy groups in the cyanate ester is in the range from 1:0.1 to about 1:2.

30. (previously presented): The method of claim 13, wherein the photoinitiator is in the range of from about 0.01 to about 20 weight percent of the composition.

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31. (previously presented): The method of claim 13, wherein the photoinitiator is selected from the group consisting of metal carbonyl complexes and ionic salts of organometallic complex cations.

32. (new): A method, comprising the steps of:

- providing a substrate including a surface thereon having a plurality of electrical conductors positioned on the surface;

- providing an integrated circuit chip located on or above the surface of the substrate and including sides, wherein a plurality of conductive leads project from respective surface portions of said sides to form an electrical path to respective portions of the surface of the substrate, and wherein a portion of said electrical path is about parallel to said surface of the substrate;

- forming a solder joint for electrically connecting each conductor with the conductor's respective lead;

- forming a composition that includes a photoinitiator, a dispersed phase of particulate silica, and a resin precursor, wherein the resin precursor consists essentially of a cyanate ester monomer, a cyanate ester prepolymer, or a mixture of the monomer and prepolymer;

- applying an amount of the composition at a thickness sufficient to cover substantially all of the solder joint; and

- photocuring the composition to reinforce the solder joint, wherein photocuring the composition forms a resin in the composition from the precursor.

33. (new): A method, comprising the steps of:

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providing a substrate including a surface thereon having a plurality of electrical conductors positioned on the surface;

providing an integrated circuit chip located on or above the substrate's surface and including sides, wherein a plurality of conductive leads project from respective surface portions of said sides, and wherein said surface portions are not about parallel to said surface of the substrate;

forming a solder joint for electrically connecting each conductor with the conductor's respective lead;

forming a composition that includes a photoinitiator, a dispersed phase of particulate silica, and a resin precursor, wherein the resin precursor consists essentially of a cyanate ester monomer, a cyanate ester prepolymer, or a mixture of the monomer and prepolymer;

applying an amount of the composition at a thickness sufficient to cover substantially all of the solder joint; and

photocuring the composition to reinforce the solder joint, wherein photocuring the composition forms a resin in the composition from the precursor.

34. (new): The method of claim 1, wherein the plurality of conductive leads project in a curved configuration toward the respective conductors.

35. (new): The method of claim 1, wherein the gap is from about 0.030 in. to about 0.050 in.

36. (new): The method of claim 1, wherein the plurality of conductive leads project a distance of

only about 0.025 in. from the respective side of the integrated chip.

37. (new): The method of claim 1, wherein the sides not including said bottom side from which the plurality of conductive leads project are curved.